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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,653	07/22/2002	Richard Spitz	10191/2277	9239

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,653	SPITZ, RICHARD	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 9-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

The electronic file only contains the heading of the Information Disclosure Statement of 3/8/02 and the Supplemental Information Disclosure Statement of 7/22/02 but no Form 1449. Therefore, Applicant is kindly requested to provide items listed Forms 1449 for both said Information Disclosure Statement and Supplemental Information Disclosure Statement.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. ***Claim 15*** recites the limitation "first and second layers" in line 2. There is insufficient antecedent basis for this limitation in the claim.

3. ***Claim 16*** recites the limitation "the layers" in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claim 16*** is rejected under 35 U.S.C. 102(b) as being anticipated by Henry et al (FR 75-24147). Henry et al teach a semiconductor component (cf. title and page 1, l. 1-10) comprising: a first layer 2 (cf. page 2, l. 26-30 and page 4, l. 5-7, from the latter it is evident that p- is an alternative to I type for region 2) of a first conductivity type (lightly doped, p- type) having a top side and a bottom side, the first layer having areas of different thickness due to at least one depression 111 (and 112; cf. page 3, l. 6-14) introduced into the top side; a second layer 3 (cf. page 2, l. 26-30) of a second conductivity type (n+ type) covering the top side of the first layer; and a third layer 1 situated on the bottom of the first layer (cf. page 2, l. 26-30), wherein the layers are diced into individual chips (along 21 and 23) (cf. Figure 1) (cf. page 2, l. 22-30), so that, in an internal area, each of the chips has at least one depression 111 or 112, and wherein the depression is sawed (cf. page 1, l. 36 – page 2, l. 3).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 9-10 and 12-15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al (FR 75 24147) in view of Rummenik (4,220,963). Henry et al introduce depressions 111 and 112 (cf. page 2, l. 15-21) into a wafer 1/2 (cf. page

2, l. 26-30; see also page 4, l. 5-7) of first conductivity type (N-type); introducing doping atoms to peripheral regions 1 and 3 on both sides of the wafer by carrying out a diffusion process (cf. page 1, l. 30-37), yielding heavily doped peripheral regions 1 and 3 (cf. Figures 2 and 3; cf. page 2, l. 26-30); dicing the wafer into individual chips (cf. page 5, l. 7-10 and Figure 1) so that, in an internal area, each of the chips has at least one depression (cf. Figures 1 and 3); and sawing the depressions (page 1, l. 37 – page 2, l. 3).

Henry et al do not necessarily teach the further limitation that the method with which the doping atoms are introduced to peripheral regions 1 and 3 comprises the steps of coating both sides of the wafer with said doping atoms and carrying out a diffusion process. However, it would have been obvious to include said further limitation in view of Rummenik, who teaches in a patent on a fast recovery diode, hence analogous art, the use of diffusion doping to create desired doped peripheral regions 11 and 12 on opposite sides of the wafer (cf. col. 2, l. 26-38). Motivation to include the method step taught by Rummenik in the method by Henry et al stems from the advantage that many wafers can be simultaneously subjected to diffusion doping through the use of a diffusion furnace. Combination of the teaching by Rummenik with the invention by Henry et al is straightforward through the use of the single heating step described by Rummenik (cf. col. 2, l. 26-38). Success in the implementation of said combination can therefore be reasonably expected.

On claim 10: the depressions 111/112 are formed as pits, having rectangular cross sections (cf. Figures 2 and 3).

On claim 12: the wafer according to the method by Henry et al is diced in areas where no depressions have been introduced (cf. page1, l. 37 – col. 2, l. 5).

On claim 13: the method by Henry further comprises the step covering a top side of the wafer using a dopant of second conductivity type (p+ type in Figure 2).

On claim 14: the method by Henry further comprises the step covering a bottom side of the wafer using a dopant of the first conductivity type (n+ type in Figure 2).

On claim 15: Henry et al teach that metal layers may be applied to both layers 1 and 3 (cf. page 3, l. 6-14) (only the metallization of 30 is actually shown, but the metallization of the bottom layer is included in the disclosure through lines 11-14 of page 3).

4. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al and Rummenik as applied to claim 9 above, and further in view of Schmid et al (5,985,067), or, in the alternative over Henry et al in view of Rummenik as applied to claim 9. Although neither Henry et al nor Rummenik disclose the further limitation of claim 11 it is inherent to a PIN diode as taught by Henry et al to have both front and back side metallization as otherwise no electrical utility is feasible; furthermore, with regard to the order of steps implied by the further limitation of claim 11, it would have been obvious to include said further limitation in view of Schmid et al, who, in a patent on a method to produce chips from a metallized wafer (cf. abstract), - hence analogous art, teaches face metallization strips 101-105 on a first main surface 112 of a wafer 100 and face metallization strips 106-110 on a second main surface of said wafer 100 (cf.

col. 8, l. 57-61), and a method of cutting the wafer that comprises the step of cutting the wafer 100 along the face metallization strips (cf. claim 5 of Schmid et al; cf. col. 9, l. 27-31; also see end result in Figure 3, with face metallization strips 130 and 131 (cf. col. 9, l. 58-61)).

Motivation to include the teaching by Schmid et al in the invention by Henry et al and Rummenik stems from the improved voltage distribution over the metallic components (cf. col. 3, l. 7-18). Combination of said teaching with said invention only requires following the same dicing technique followed by Schmid et al and in no way interferes with the remainder of the invention by Henry et al and Rummenik. Success of the implementation of said combination can therefore be reasonably expected.

In the alternative rejection over merely Henry et al and Rummenik, Applicant is reminded of Ex Part Rubin, 128 USPQ 440 (Bd. App. 1959) (Prior Art disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious). Consequently, in view of the absence of any teaching in Applicant's disclosure as to the critical nature of the order in which the metallization and the cutting steps are to be performed the further limitation of claim 11 thus only reduces to the application of metal layers to both sides of the wafer, which is inherent in any PIN diode.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Tursky et al (DE 41 35 258 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
September 29, 2003